

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

Eliyahou Harari et al.

Title:

Multi-State Non-Volatile Integrated Circuit Memory Systems That

Employ Dielectric Storage Elements

Application No.:

10/002,696

Filing Date:

October 31, 2001

Examiner:

Weiss, Howard

Group Art Unit:

2814

Docket No.:

SNDK.272US0

Conf. No.:

4652

Mail Stop RCE Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicants call the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application. Copies of the documents listed on the accompanying Form PTO-1449 are enclosed.

Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

This information disclosure statement is submitted under 37 C.F.R. § 1.97(b) and consequently no fee should be required. The Commissioner is authorized, however, to charge

Attorney Docket No.: SNDK.272US0

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any fee that may be required, or to credit any overpayment, against Deposit Account No. 502664, as set forth in the accompanying Transmittal Letter.

EXPRESS MAIL LABEL NO.:

EV437667615US

Respectfully submitted,

Gerald P. Parsons

Reg. No. 24,486

April 6, 2004

Date

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U.S. Department of Commerce, Patent and Trademark			Atty. Docket No.			Application No.		
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	12	Process for Produ	cing Said Memor	platile Electrically Erasa ry Structure and Method n 60/296,618, filed June	ls for Program	ming and Erasi	ng Said Mei	mory
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